## IN THE CLAIMS:

Please amend the claims as follows:

1. Amended) A [semiconductor device] <u>ferroelectric liquid crystal display device</u> having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said [semiconductor device] <u>CMOS circuit</u> comprising:

each gate electrode of said n-channel TFT and said p-channel TFT [has] <u>having</u> a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with both said first conductive layer and said gate insulating film;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said first impurity region of said n-channel TFT is disposed so as to [completely]

partially overlap[s] with [said second conductive layer] a portion of said second conductive layer

which is in contact with said gate insulating film;

wherein said third impurity region of said p channel TFT is disposed so as to partially [overlap[s]] with [said second conductive layer] another portion of said second conductive layer which is in contact with said gate insulating film.

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## Please add following claims.

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Af 2. A ferroelectric liquid crystal display device according to claim 1, wherein said first conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

#-3. A ferroelectric liquid crystal display device according to claim 1, wherein each of said first conductive layers of said n-channel TFT and said p-channel TFT comprises a single layer or a plurality of layers.

4. A ferroelectric liquid crystal display device according to claim 1, wherein said second conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo). ♦

impurity region is a LDD region, said second impurity region is a source or a drain region, and said third impurity region is the source or the drain region.

A ferroelectric liquid crystal display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with both said first conductive layer and said gate insulating film;

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region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said first impurity region of said n-channel TFT is disposed so as to partially

/ 2 [overlaps] with a portion which said second conductive layer is in contact with said gate insulating film;

wherein said second impurity region of said n-channel TFT is disposed so as not to hyer

[overlaps] with said second conductive film;

wherein said third impurity region of said p-channel TFT is disposed so as to partially [overlaps] with said portion which said second conductive layer is in contact with said gate insulating film.

cont.

- 8-7. A ferroelectric liquid crystal display device/according to claim 6, wherein said first conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo). ♣
- e-8. A ferroelectric liquid crystal display device according to claim 6, wherein each of said first conductive layers of said n-channel TFT and said p-channel TFT comprises a single layer or a plurality of layers.

4-9. A ferroelectric liquid crystal display device according to claim 6, wherein said second conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).-

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10. A ferroelectric liquid crystal display device according to claim 6, wherein said first impurity region is a LDD region, said second impurity region is a source or a drain region, and said third impurity region is the source or the drain region.

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A ferroelectric liquid crystal display device having an n-channel TFT and a p-channel TFT over a substrate,

said n-channel TFT comprising:

A2 Cunt. a first gate electrode formed adjacent to a first semiconductor layer with a first gate insulating film interposed therebetween, said first semiconductor layer comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region;

wherein said first impurity region is disposed so as to partially overlaps with said first gate electrode, and

said p-channel TFT comprising:

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a second gate electrode formed adjacent to a second semiconductor layer with a second gate insulating film, said second semiconductor layer comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

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wherein said third impurity region is disposed so as to partially overlaps with said

second gate electrode.

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and second gate/electrode/comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).-

A13. A ferroelectric liquid crystal display device according to claim 11, wherein said first impurity region is a LDD region, said second impurity region is a source or a drain region, and said third impurity region is the source or the drain region.

and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with both said first conductive layer and said gate insulating film;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said first impurity region of said n-channel TFT is disposed so as to partially [overlaps] with a portion which said second conductive layer is in contact with said gate insulating film;

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wherein said third impurity region of said p-channel TFT is disposed so as to partially [overlaps] with said portion which said second conductive layer is in contact with said gate insulating

film.#

15. A goggle type display device according to claim 14, wherein said first conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

a-16. A goggle type display device according to claim 14, wherein each of said first conductive layers of said n-channel TFT and said p-channel TFT comprises a single layer or a plurality of layers.

417. A goggle type display device according to claim 14, wherein said second conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

region is a LDD region, said second impurity region is a source or a drain region, and said third impurity region is the source or the drain region.

and a p-channel TFT, said CMOS circuit comprising:

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cach gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with both said first conductive layer and said gate insulating film;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said first impurity region of said n-channel TFT is disposed so as to partially [overlaps] with a portion which said second conductive layer is in contact with said gate insulating film;

wherein said second impurity region of said n-channel TFT is disposed so as not to layer overlaps with said second conductive film;

wherein said third impurity region of said p-channel TFT is disposed so as to partially

| Toverlaps | with | said | portion which said second conductive layer is in contact with said gate insulating film.

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e-20. A goggle type display device according to claim 19, wherein said first conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo). ♣

- #21. A goggle type display device according to claim 19, wherein each of said first conductive layers of said n-channel TFT and said p-channel TFT comprises a single layer or a plurality of layers.
  - 4-22. A goggle type display device according to claim 19, wherein said second conductive layers of said n-channel TFT and said p-channel TFT comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

region is a LDD region, said second impurity region is a source or a drain region, and said third impurity region is the source or the drain region.

A goggle type display device having an n-channel TFT and a p-channel TFT over a substrate,

said n-channel TFT comprising:

a first gate electrode formed adjacent to a first semiconductor layer with a first gate insulating film interposed therebetween, said first semiconductor layer comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region;

wherein said first impurity region is disposed so as to partially overlaps with said first gate electrode, and

said p-channel TFT comprising:

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a second gate electrode formed adjacent to a second semiconductor layer with a second gate insulating film, said second semiconductor layer comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said third impurity region is disposed so as to partially overlaps with said

second gate electrode.

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#25. A goggle type display device according to claim 24, wherein said first and second gate electrode comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

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4-26. A goggle type display device according to claim 24, wherein said first impurity region is a LDD region, said second/impurity region is a source or a drain region, and said third impurity region is the source or the drain region.

## **REMARKS**

## I. <u>Title</u>

In the Office Action, the Examiner objects to the title of the invention as not being descriptive. Accordingly, Applicants are amending the title to recite -- Ferroelectric Liquid Crystal and Goggle Type Display Devices -- , which is consistent with the claims herein. Therefore, it is requested that this rejection be withdrawn.